
SECTION III

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SAMPLE AND HOLDS/ TRACK AND HOLDS

A sample-and-hold amplifier (SHA) is a device that has a signal input, a signal output, and a control input. As the name implies, a SHA has two steady-state operating modes. In the sample (or track) mode, the output tracks the input as faithfully as possible until the hold command is applied to the control input. In the hold mode, the output retains the last value of the input signal that it had at the instant of time the hold command was applied.

By far the largest application for SHAs is driving A/D converters. SHAs are essential for successive approximation or subranging A/D converters where the signal input to the A/D converter must remain stable within 1/2 LSB during the conversion cycle. Significant dynamic performance improvements can sometimes be realized by placing a fast SHA ahead of a flash converter. Other applications for SHAs are:

D/A converter deglitchers, simultaneous sampling systems, peak detectors, pulse stretchers, delay lines, and data distribution systems.

Most track and holds and sample and holds are identical in both function and circuit implementation. The only distinction between them is how they are used in the system. A sample and hold implies that the device samples the input for a short time and stays in the hold mode for the remainder of the cycle. A track and hold, on the other hand, spends most of the time tracking the input and is switched into the hold mode for only brief intervals. In data acquisition systems operating at sampling rates greater than 1 MHz, the terms sample and hold and track and hold lose their distinction. In the following discussion the terms will therefore be used interchangeably.

SAMPLE-AND-HOLD APPLICATIONS

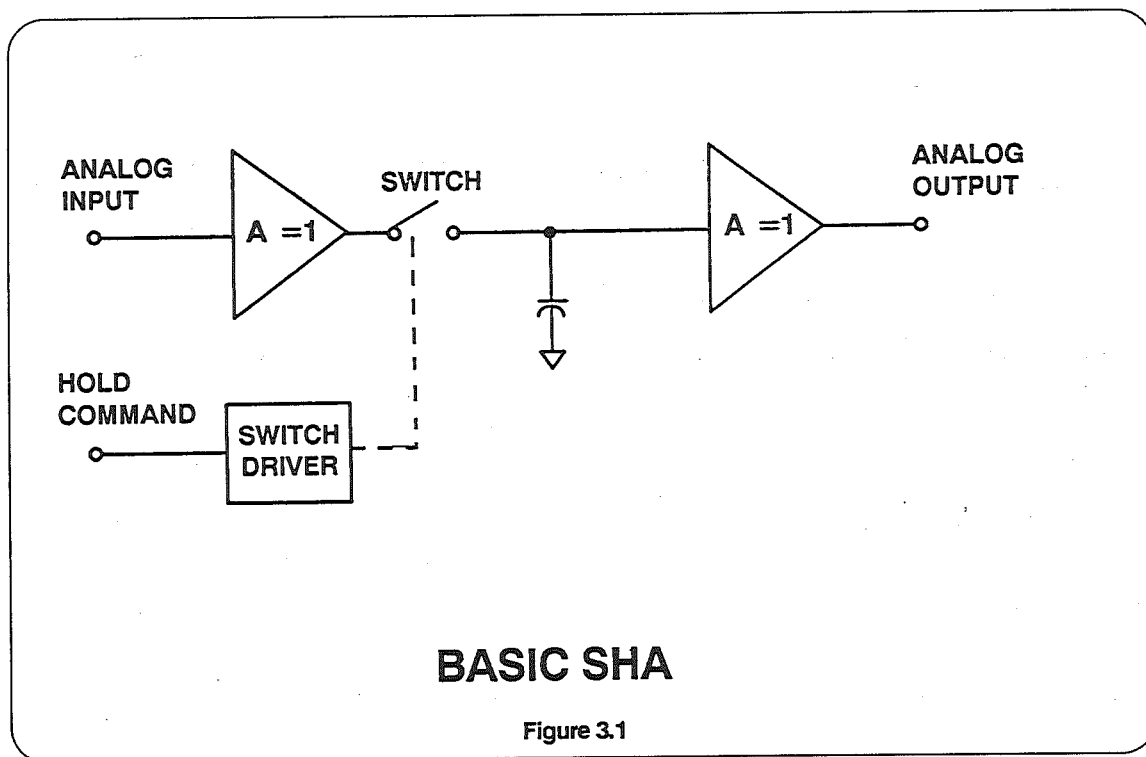
- **A/D Converter Drivers**
- **D/A Converter Deglitchers**
- **Data Acquisition Systems**
- **Data Distribution Systems**
- **Simultaneous Sampling**
- **Peak Detectors**
- **Analog Delay Lines**

BASIC SHA OPERATION

Regardless of the circuit details or type of SHA in question, all such devices have four major components. The input amplifier, energy storage device (hold capacitor), output buffer, and switching circuits are common to all SHAs, as shown in the typical configuration of Figure 3.1.

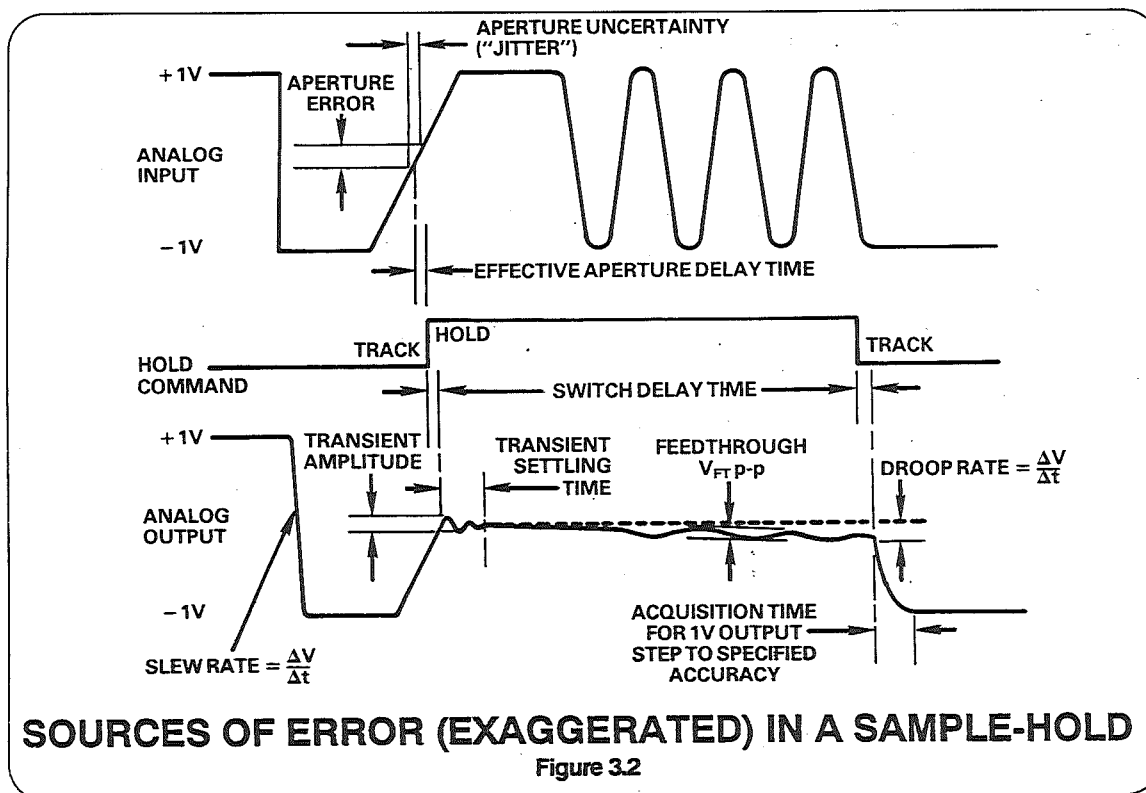
The energy-storage device, the heart of the SHA, is almost always a capacitor. The input amplifier buffers the input by presenting a high impedance to the signal source and providing current gain to

charge the hold capacitor. In the track mode, the hold capacitor usually determines the frequency response of the device; in the hold mode, the capacitor retains the voltage present before it was disconnected from the input buffer. The output buffer offers a high impedance to the hold capacitor to keep the held voltage from discharging prematurely. The switching circuit and its driver form the mechanism by which the hold capacitor is alternately switched between track and hold.



There are four groups of specifications that properly describe SHA operation. They are the static and dynamic characteristics that describe operation in and between the track and hold modes. Unique to SHAs are the dynamic specifications that describe the transitions from

track to hold, and hold to track. An understanding of the terminology used to describe these devices is of key importance to the proper selection and use of SHAs. Figure 3.2 shows errors (exaggerated) during a complete cycle from track to hold and back.



TRACK MODE SPECIFICATIONS

While in the track - or sample - mode of operation, the SHA is simply a limited-bandwidth amplifier that may or may not provide gain. Operation in this mode is described by the same specifications that are used to characterize any analog amplifier. Indeed, many SHAs are little more than an operational amplifier with a capacitor and a switch. The principal specifications used to describe sample-mode operation are:

OFFSET - That error which adds to the actual input to displace the transfer characteristics of the SHA from the ideal. It is usually measured referred to the input.

NONLINEARITY - The amount by which the plot of output vs. input deviates from a "best straight line". It is usually specified as a percentage of full scale.

GAIN - The multiplication factor describing the input to output DC transfer function.

SETTLING TIME - The time required for the output to attain its final value within a specified fraction of full scale when a full scale analog input step is applied.

BANDWIDTH - Describes the frequency response in terms of output attenuation over frequency; it is usually characterized by the -3 dB value.

SLEW(ING) RATE - The maximum rate of change of the output voltage when an analog step is applied, either as an input step or by a hold-to-sample transition.

TRACK-TO-HOLD TRANSITION SPECIFICATIONS

The specifications used to describe the transition from track to hold and from hold to track seem to be the most confusing to users of SHAs. These terms are unique to SHA devices and deserve special attention. Perhaps the most misunderstood and misused specifications are those that include the word "aperture" in their definition.

APERTURE TIME - The most essential dynamic property of a SHA is its ability to quickly disconnect the hold capacitor from the input buffer amplifier. The short (but non-zero) interval required for this action is called aperture time. The actual value of voltage that gets held at the end of this interval is a function of both the input signal and the errors introduced by the switching operation itself.

SAMPLE-TO-HOLD OFFSET OR PEDESTAL

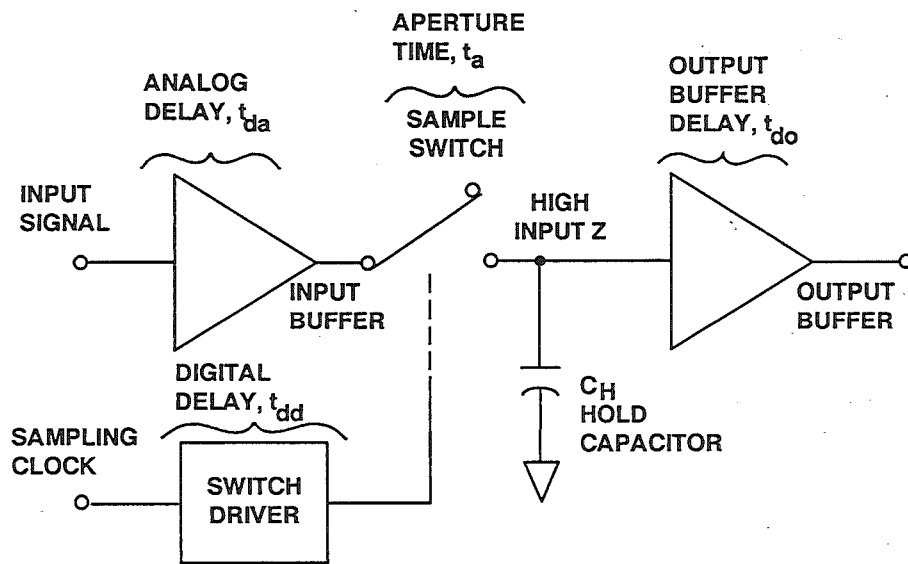
There is a step error, which causes the held value to differ from the last value in sample; it is caused by charge dumped onto the hold capacitor via stray capacitance from the switch-control circuit. A design objective is to keep this error, resulting from a non-ideal switch, independent of the input signal level; the degree to which it in fact deviates from a constant over the input signal range can result in nonlinearities in the output with respect to the input signal. The constant offset portion of the error, called charge transfer, or offset step, can be compensated by coupling a signal of opposite phase onto the hold capacitor through an auxiliary switching circuit and compensation capacitor.

Thus, the sample-to-hold offset, or pedestal, specification depends on the actual

device configuration. For SHAs having fixed internal hold capacitance, it includes the residual uncorrected step and the offset nonlinearity. For SHAs requiring external capacitors, it is the residual step error after the charge transfer is accounted for and/or cancelled. In a device for which the capacitance can be chosen by the user, these effects can be reduced by increasing the capacitance in proportion, but at the cost of increased acquisition time.

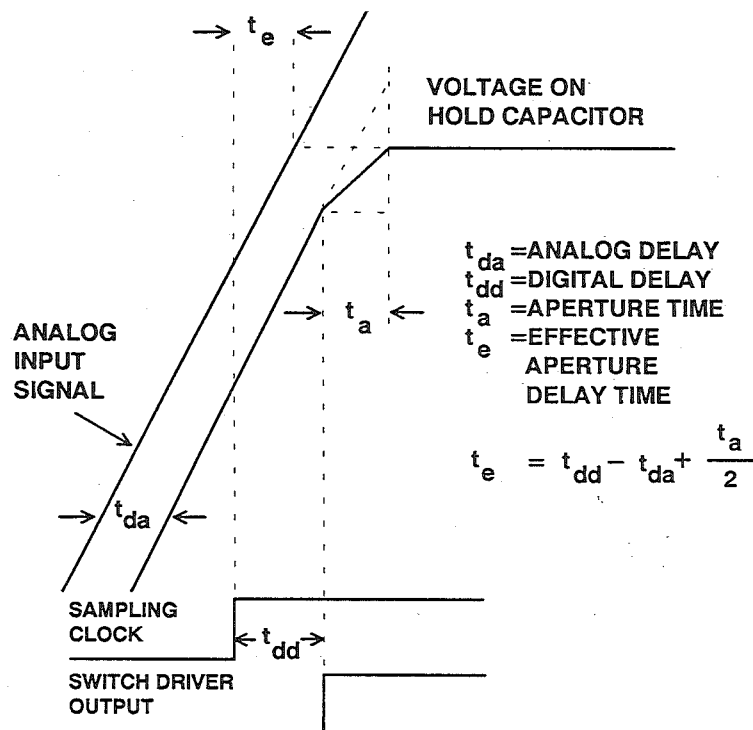
APERTURE DELAY (Or, more descriptively, **EFFECTIVE APERTURE DELAY TIME**) - This specification is important because it helps the SHA user know when to strobe the device with respect to the input signal timing. Figure 3.3 shows the sequence of what happens when the hold command is applied with an input signal of arbitrary slope (for clarity, the sample to hold offset error and switching transients are ignored). The value that finally gets held is a delayed version of the input signal, averaged over the aperture time of the switch. Effective aperture delay time is defined as the interval between the leading edge of the hold command and the instant when the input signal was equal to the held value. This is a more useful specification than aperture time alone, because it includes the effects of the analog and digital propagation delays, as well as the aperture time.

The formula in Figure 3.4 is based on the assumption that the value of voltage on the hold capacitor is approximately equal to the average value of the signal applied to the switch over the interval during which the switch changes from a low to high impedance (aperture time).



IDEALIZED SAMPLE-AND-HOLD CIRCUIT

Figure 3.3



SAMPLE-AND-HOLD WAVEFORMS

Figure 3.4

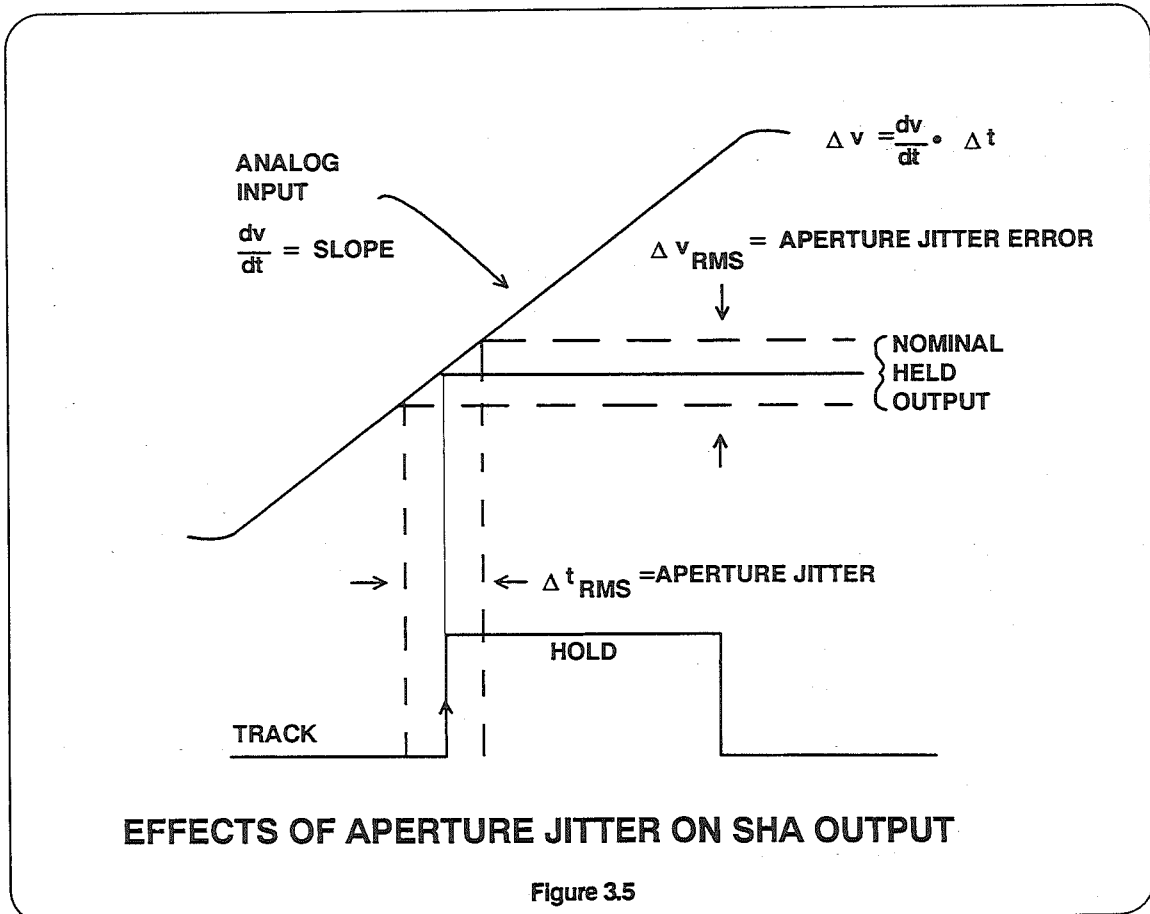
APERTURE UNCERTAINTY (JITTER) - Aperture uncertainty, or "jitter", is the result of noise which modulates the phase of the hold command. This jitter shows up as a sample to sample variation in the value of the analog signal which is being "frozen".

Aperture uncertainty manifests itself as an aperture error, as shown in Figure 3.5. The amplitude of the error is related to the rate of change of the analog input. For any given value of aperture uncertainty, aperture error will increase as the input dv/dt increases.

SWITCHING TRANSIENT - As shown in Figure 3.2, most SHA specifications include

the maximum amplitude and duration of the transient that appears at the output as a result of the sample-to-hold transition. A similar transient appears during the hold-to-sample transition but is usually not noticeable because of the dominant effect of acquisition time.

SWITCH DELAY TIME - The interval between the edges of the hold command and the beginning of change of state at the analog output. This delay, as shown in Figure 3.2, occurs at both the sample-to-hold and hold-to-sample transition.



HOLD MODE SPECIFICATIONS

During the hold mode there are errors due to imperfections in the switch, the output amplifier, and the hold capacitor.

DROOP - A constant drift of the output voltage due to charge leakage from the hold capacitor through the switch, output buffer, circuit board or substrate - or within the capacitor itself ($dV/dt = I/C$). This error can be reduced by increasing the hold capacitance (at the cost of increased acquisition time) and/or reducing leakage currents by component choice, component placement, and shielding or guarding. When droop is caused by diode leakage currents it will double with every 10°C temperature rise.

FEEDTHROUGH - The fraction of input signal that appears at the output in hold,

caused primarily by capacitance across the switch. Usually measured by applying a full scale sinusoidal input at a fixed frequency (e.g., 20V peak to peak at 10 MHz) and observing the output during hold.

DIELECTRIC ABSORPTION - The tendency of charges within a capacitor to redistribute themselves over a period of time, resulting in "creep" to a new level when allowed to rest after large, fast changes. This effect, less than 0.01% for good polystyrene and teflon capacitors, can be as large as several percent for ceramic and mylar capacitors. Dielectric absorption can therefore become the dominant error in SHAs when care is not taken with the choice of the capacitor.

HOLD TO TRACK TRANSITION SPECIFICATIONS

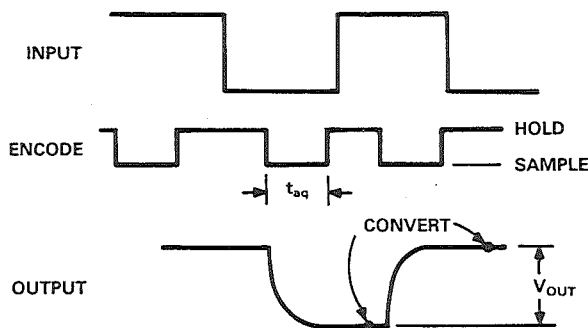
ACQUISITION TIME - The length of time during which the SHA must remain in the sample mode in order for the hold capacitor to acquire a full scale step input; adequate acquisition time makes it possible for the subsequent hold mode output to be within a specified error band of the final value.

Acquisition time is a key SHA dynamic specification. The maximum sample rate of any SHA is limited by the sum of the time intervals required for the sample and the hold modes. The interval spent in the hold mode (after transients have settled) is primarily determined by the system in which the SHA is used. The minimum time spent in the sample mode, however, is established by the sample hold's acquisition time for a given degree of accuracy.

When acquisition time is measured as the interval from the hold to sample transition to the instant when the output buffer has settled, the resulting value of acquisition time is generally pessimistic. As defined, acquisition time measures the time required to acquire the signal at the hold capacitor, not necessarily at the output of the buffer (unless they are the same). For devices in which the hold capacitor is buffered by a follower, rather than used as an integrator (see the next section), a measurement at the output includes output buffer settling time as well as switch delay time. In practice, the voltage has already settled at the hold capacitor, and a hold command can be applied before the output buffer completely settles.

There is a method of determining acquisition time which is independent of output buffer effects. Figure 3.6 shows the waveforms involved. The input analog square wave is sampled and converted at twice the analog square wave frequency with relatively narrow sample pulses. The figure indicates that, on the transition to sample, the output starts to change, in order to follow the step input. Initially set wide enough for the signal to be accurately acquired, the pulsewidth, t_{aq} , is

reduced until the output waveform measured directly, begins to collapse to some defined percentage of full scale. When that occurs, the width of the sample pulse is equal to the acquisition time, because the hold capacitor can no longer acquire the signal accurately with further reduction in t_{aq} . If the output is being observed with an oscilloscope, it is possible to make this measurement on high vertical sensitivity settings even if the scope is being overdriven severely.



ACQUISITION-TIME MEASUREMENT WAVEFORMS

Figure 3.6

SAMPLE AND HOLD SPECIFICATIONS

TRACK MODE

STATIC

- Offset
- Nonlinearity
- Gain

DYNAMIC

- Settling Time
- Bandwidth
- Harmonic Distortion
- Slew Rate

TRACK TO HOLD TRANSITION

STATIC

- Pedestal
- Pedestal Nonlinearity

DYNAMIC

- Switch Aperture Time
- Effective Aperture Delay Time
- Aperture Jitter
- Switch Delay Time
- Switching Transient

HOLD MODE

STATIC

- Droop
- Dielectric Absorption

DYNAMIC

- Feedthrough

HOLD TO TRACK TRANSITION

DYNAMIC

- Acquisition Time
- Switching Transient

HIGH SPEED OPEN LOOP SHAS

Most SHA designs fall into one of two categories: open or closed loop circuits. Closed loop SHAs exploit the accuracy, low drift, and gain flexibility available with operational amplifiers. Open loop designs take advantage of the high speed characteristics of unity gain buffer amplifiers.

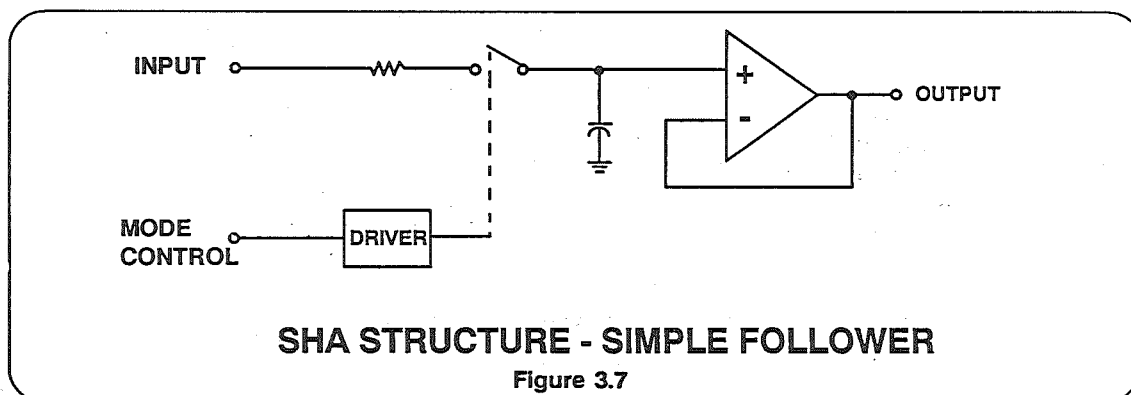
Figure 3.7 shows the conceptually simplest SHA circuit. When the switch is closed, the capacitor charges exponentially to the input voltage, and the amplifier's output follows the capacitor's voltage. When the switch is opened, the charge remains on the capacitor. The capacitor's acquisition time depends on the series resistance and the current available to charge the capacitor. Once the charge is acquired to the appropriate accuracy, the switch can be opened, even though the amplifier has not yet settled, without affecting the final output value.

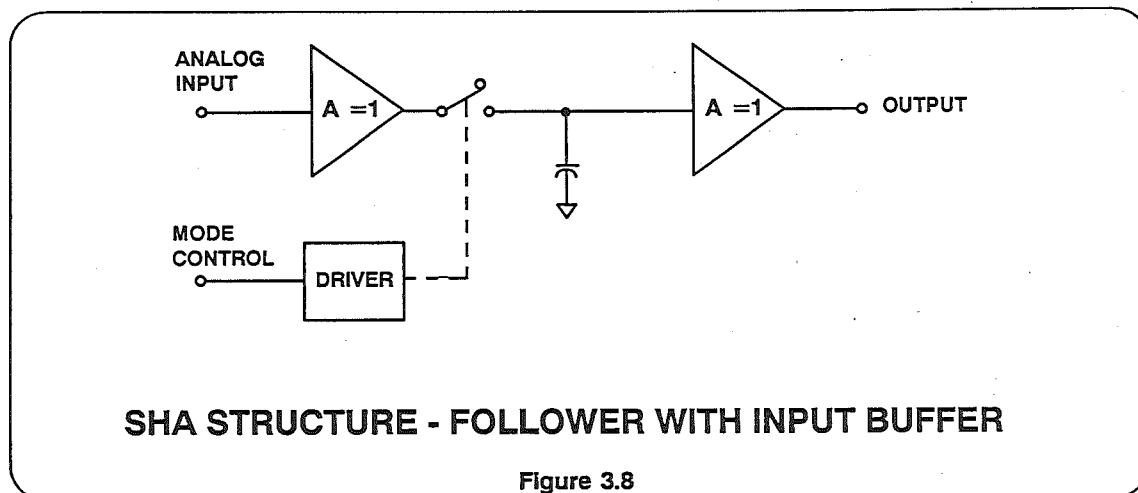
A disadvantage of this circuit is that the switched capacitor dynamically loads the input source, which may not have low enough output impedance and sufficient current-drive capacity. The circuit of Figure 3.8 is similar but includes an input buffer amplifier to isolate the source. The Analog Devices HTS-0025 and HTS-0010 SHAs use this scheme to achieve acquisition

times as low as 10ns. These designs utilize a high speed diode switching bridge for sampling wide bandwidth signals at update rates of up to 50 MHz as shown in Figure 3.9. The high speeds are achieved by employing buffer amplifiers that do not use voltage feedback; the nonlinearities of these amplifiers limit their use to systems requiring resolutions of 12 bits or less.

The HTS-0010 is an example of a SHA that has the hold capacitor's active terminal brought out so that additional capacitance can be employed to improve the droop rate and sample-to-hold offset (at the expense of bandwidth and acquisition time, as noted earlier).

SHA specifications and terminology are generally applicable to both open loop and closed loop SHAs. Applications requiring update rates higher than 10 MHz and acquisition times less than 100ns usually require open loop circuits. At these speeds, subtle distinctions in terminology can mislead the system designer. Before selecting a high speed SHA, the user should have a clear understanding of the intent and meaning of the manufacturer's usage of such specifications as aperture time and acquisition time.



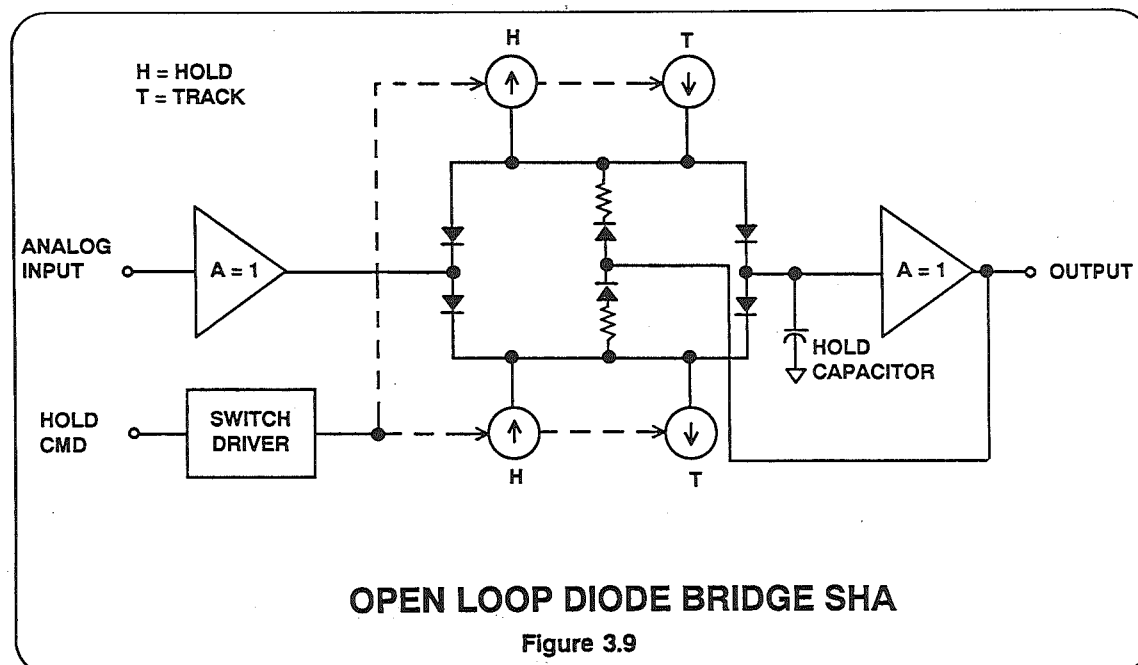


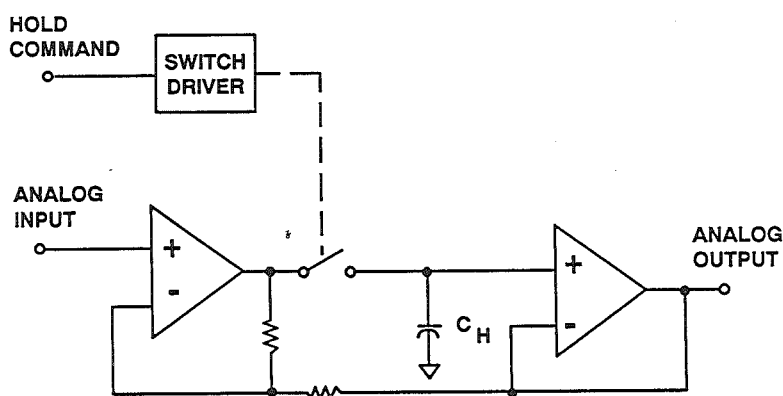
CLOSED LOOP SHAS

The circuit of Figure 3.9 has the essential advantage of potentially fast acquisition and settling time because it is an open loop device.

If low frequency tracking accuracy is more important than speed, this can be accomplished by closing the loop around the storage capacitor and using high loop gain to enforce tracking accuracy.

Figure 3.10 shows a configuration in which the input follower of Figure 3.9 is replaced by a high gain difference amplifier. Now, when the switch is closed, the output (which represents the charge on the capacitor) is forced to track the input, within the capability of input amplifier's gain, bandwidth, common-mode error, and current driving capabilities. SHAs using this circuit configuration to achieve





**SHA STRUCTURE -
FEEDBACK CIRCUIT WITH OUTPUT FOLLOWER**

Figure 3.10

higher accuracy than that available in open loop circuits include the Analog Devices AD582, AD583 and ADSHC-85.

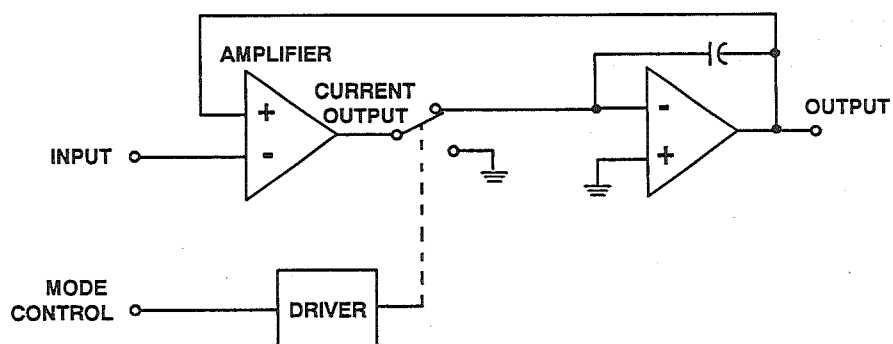
In Figure 3.11 (which illustrates the architecture of the closed loop AD585 and SHA1144), an integrator configuration is used to charge the capacitor, permitting the switch to operate at ground potential; this simplifies leakage problems.

Because both the output and the input affect the charge on the capacitor, the acquisition time and the settling time are identical in the circuits of both Figure 3.10 and 3.11. If the circuit of Figure 3.10 is switched into hold before the output has settled at its final value, the sample may be in error. In addition, since the loop is open during hold, the input stage must reacquire the input when the circuit is returned to sample, even if the input is unchanged. As a rule, this will result in a spike if the input amplifier has high voltage gain.

If input impedance and acquisition time are not critical, and sufficient drive current is available from the source, the circuit of Figure 3.12 may be desirable.

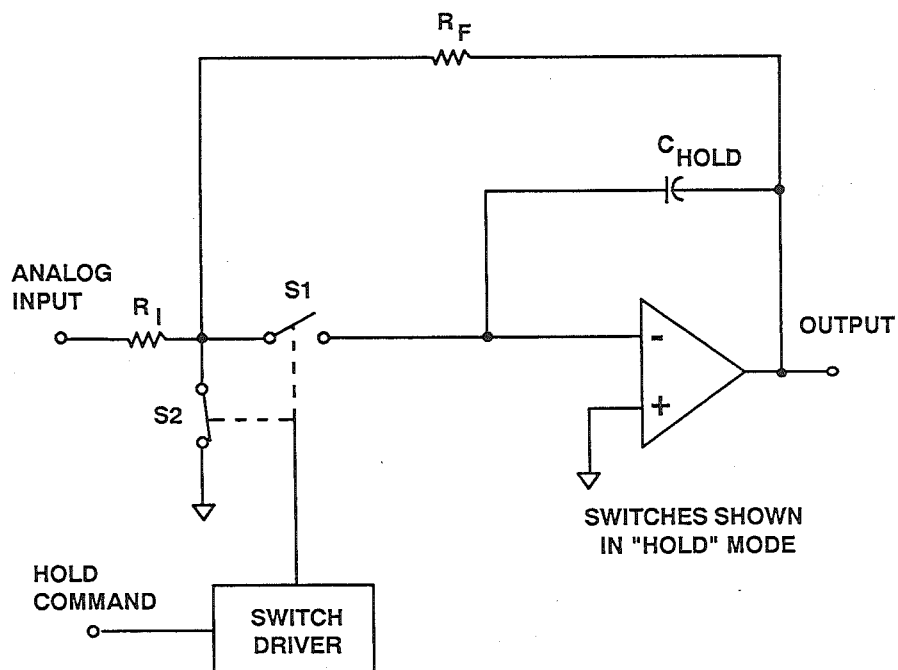
Here, only a single operational amplifier is required; and the input impedance and gain are a function of the choice of R_i and R_f . In both sample and hold, the input impedance to ground is R_i . In the sample mode, the input circuit sees a virtual ground through R_i and the hold capacitor is charged by the amplifier. In the hold mode, the resistance mode is switched to analog ground potential to disconnect the capacitor while minimizing signal feedthrough and maintaining a constant input impedance. The Analog Devices AD346, AD389 and HTC-0300A all utilize this principle. The circuit of Figure 3.13 takes advantage of the common mode rejection of the op-amp to minimize charge injection and is implemented in the HTC-0300A design.

SHAs are most widely used in data acquisition systems, typically as shown in Figure 3.14. The SHA maintains the input to the A/D converter constant during the conversion interval; meanwhile, the multiplexer is seeking the next channel to be converted, either randomly or sequentially. As soon as conversion is completed, the SHA samples the newly established input, and the cycle is repeated.



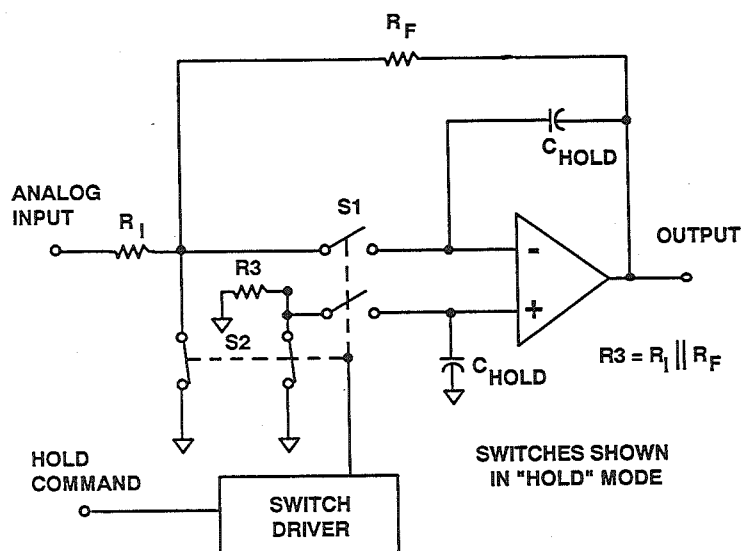
**SHA STRUCTURE -
FEEDBACK CIRCUIT WITH OUTPUT INTEGRATOR**

Figure 3.11



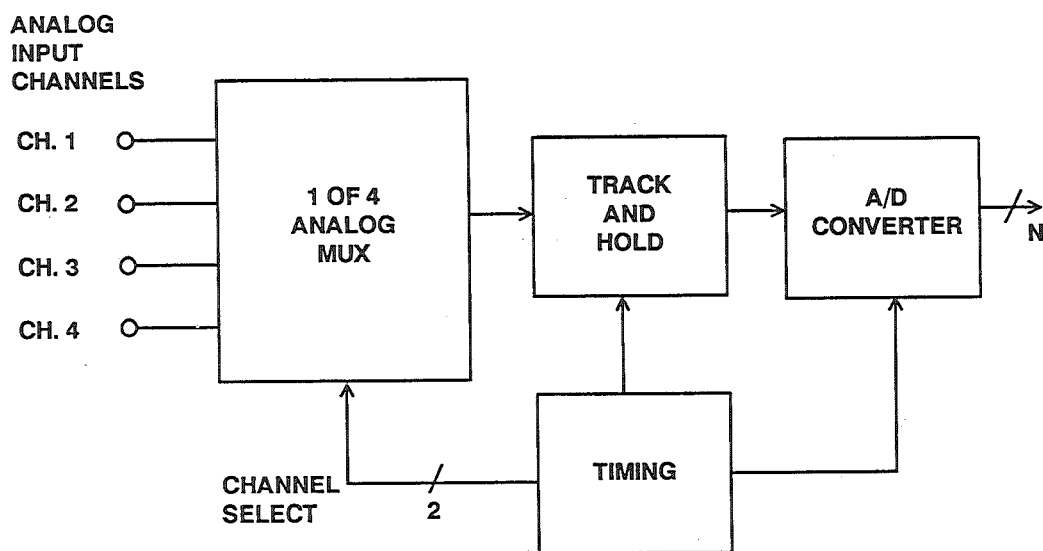
**SHA STRUCTURE - INVERTING INTEGRATOR
SWITCHED AT SUMMING POINT**

Figure 3.12



DIFFERENTIAL SWITCHING TO REDUCE CHARGE INJECTION

Figure 3.13



TRADITIONAL DATA ACQUISITION SYSTEM USING ANALOG MULTIPLEXER

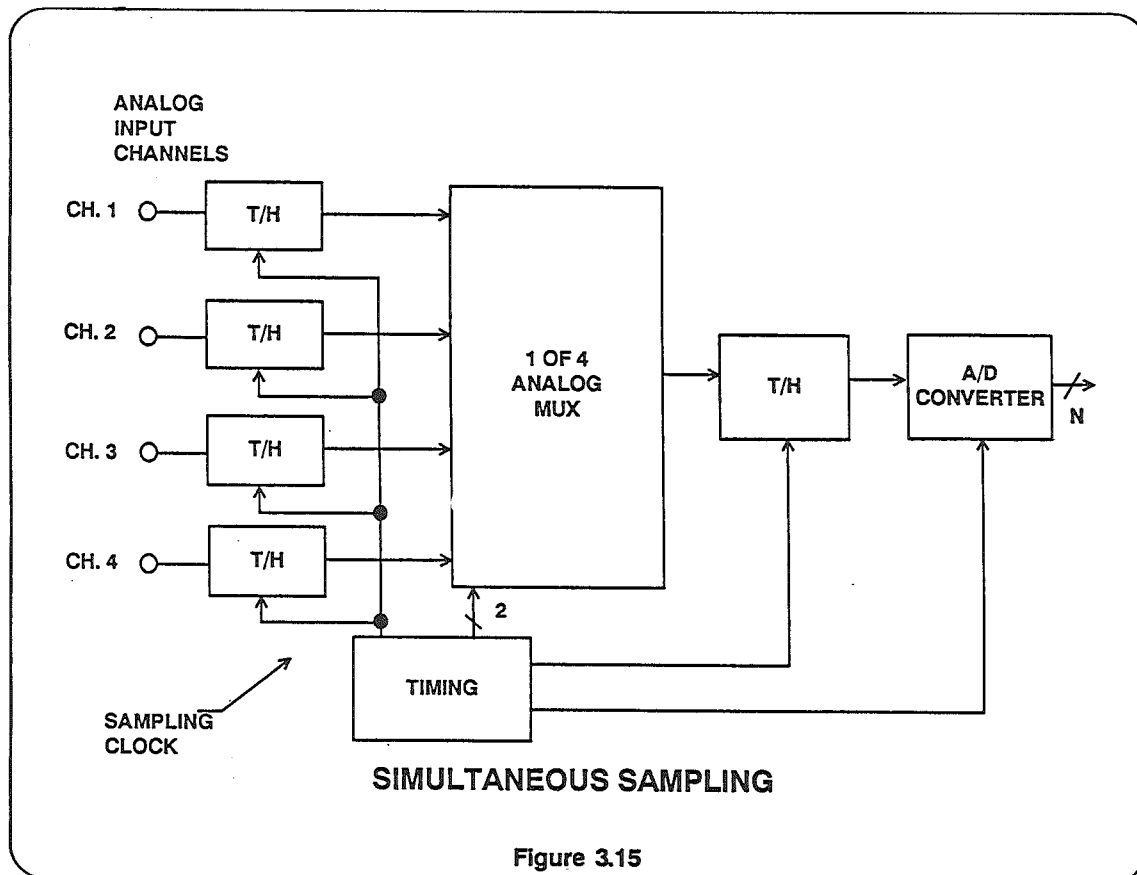
Figure 3.14

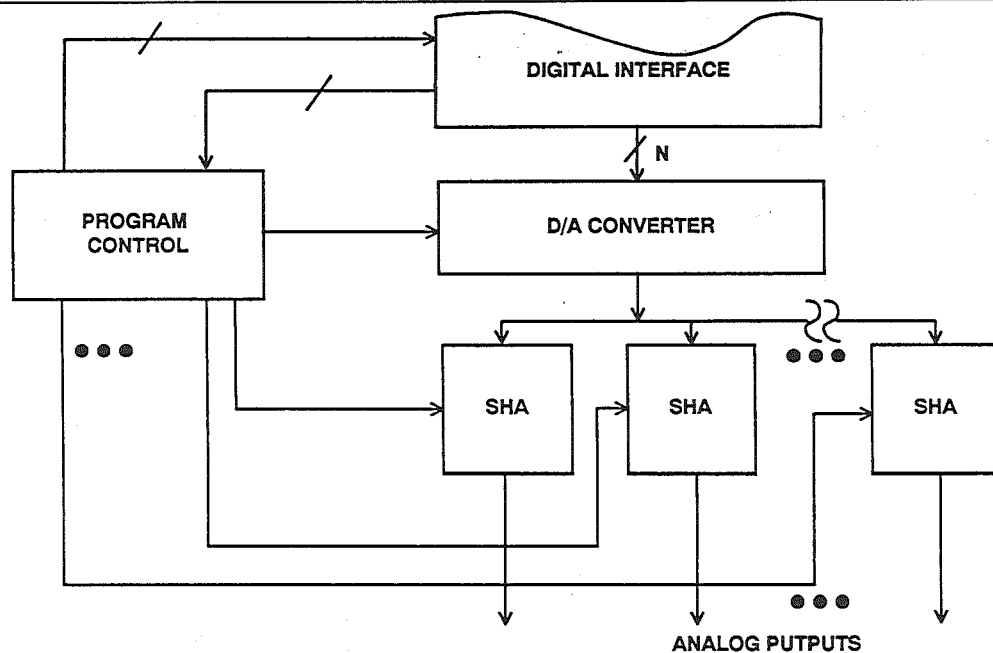
This mode of operation is known as synchronous sampling; the sample-hold operates in synchronism with the other system elements. In another mode (viz., asynchronous), a large number of SHAs may be used to acquire and store data at rates pertinent to each individual channel. They are then either interrogated by analog multiplexers as shown in Figure 3.15, or the signals are individually converted asynchronously, and then multiplexed digitally.

In data distribution, 0.01% SHAs may be less costly than large number of D/A converters having comparable accuracy. A typical data distribution system is shown in Figure 3.16. A fast, accurate D/A converter updates a number of sample-holds at speed and accuracy levels appropriate to the individual channels.

Sample-holds are also used to deglitch D/A converters in systems that are sensitive to the D/A glitches that occur at transition points. Figure 3.17 shows the timing relationship used when deglitching DACs. Just prior to latching the new data into the D/A converter, the SHA is put into the hold mode, so that D/A glitches are isolated from the output. SHAs used as deglitchers must have very small sample-to-hold and hold-to-sample transients and pedestal errors, as well as fast acquisition times.

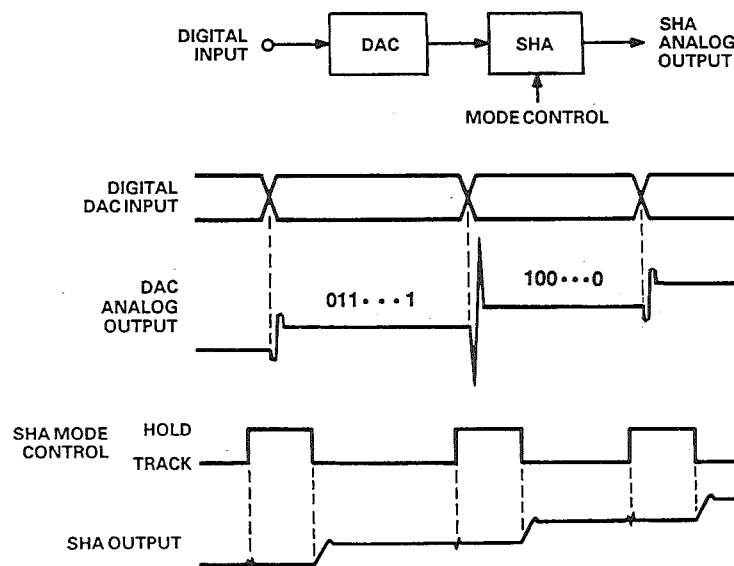
Another application of the SHA is a peak detector. A typical example is shown in Figure 3.18. When the input is greater than the SHA output, the comparator's positive output causes the SHA to track.





**DATA DISTRIBUTION SYSTEM USING
SINGLE D/A AND MULTIPLE SHAS**

Figure 3.16



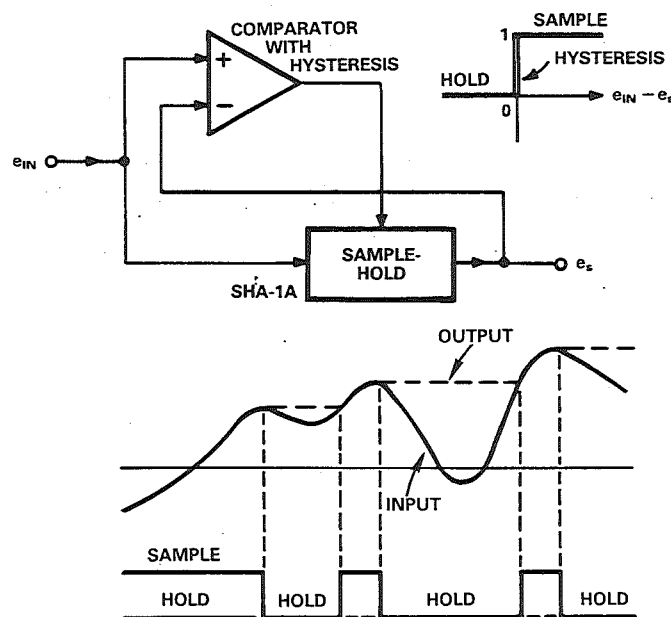
DEGLITCHING THE OUTPUT OF A D/A CONVERTER

Figure 3.17

When the input decreases and becomes less than the SHA output, the comparator's 0 output causes the SHA to hold until the input again becomes greater than the output. To reset, the control input is arbitrarily switched into Sample, and the lowest expected level is applied at the input. The SHA output (or the comparator input) is biased by a few millivolts of hysteresis to avoid ambiguity during

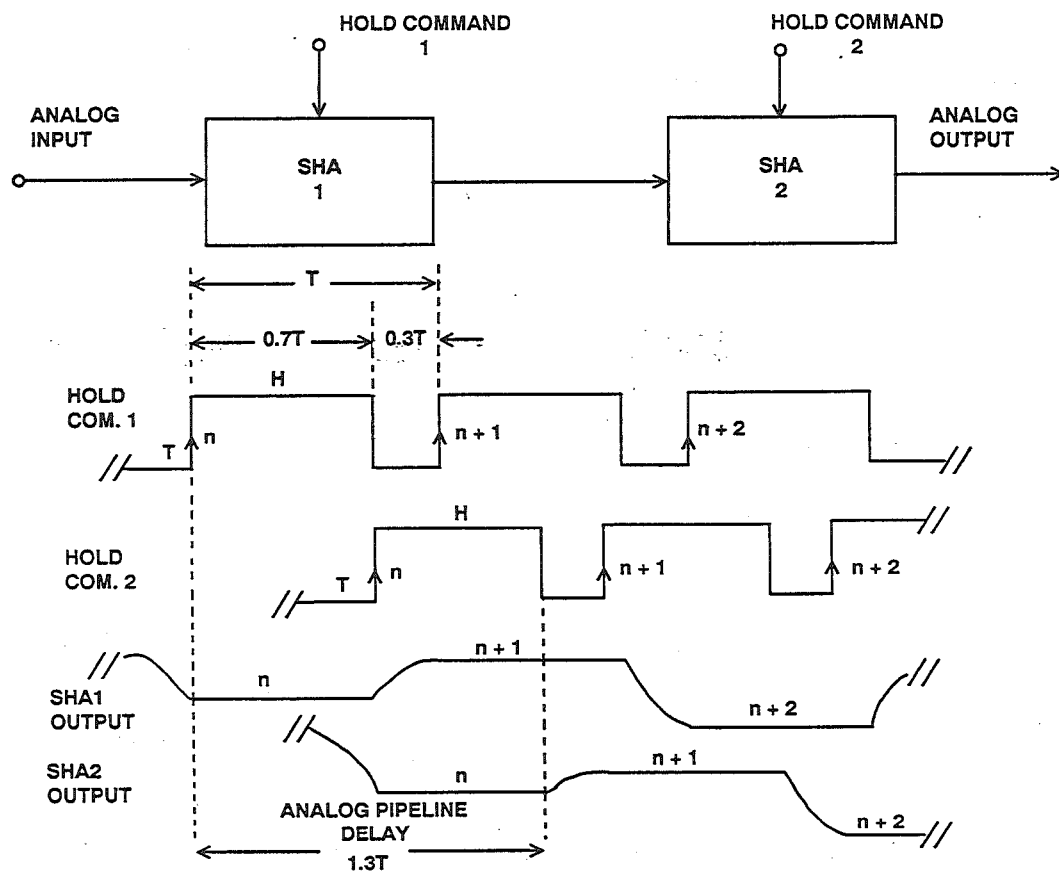
step inputs and minimize false triggering by noise.

Multiple SHAs can be used in series to generate analog delays as shown in Figure 3.19. SHA 2 is placed in hold just prior to the end of the hold interval for SHA 1. This results in a pipeline delay greater than the sampling period.



PEAK FOLLOWER, USING A SHA AND A COMPARATOR

Figure 3.18



SHAS USED FOR ANALOG PIPELINE DELAY

Figure 3.19

DRIVING FLASH CONVERTERS WITH HIGH SPEED SHAS

Significant improvements in the dynamic performance (ENOBs, SNR, harmonic distortion) of flash converters can sometimes be obtained by the proper use of SHAs as drivers. As has been discussed previously in the section on A/D converters, flash converter dynamic performance is often limited by the effective sampling time delay matching between the comparators in the comparator bank. By placing the appropriate SHA ahead of the flash converter as shown in Figure 3.20, the input to the flash converter can be made to appear as a DC value. The usefulness

of this technique is limited to sampling rates of less than 50 MHz if discrete components must be used. Beyond 50 MHz, the SHA and the flash converter should be integrated into a carefully designed single circuit in order to avoid limitations due to parasitics associated with a package and interconnections.

The task of matching a SHA to a flash even at sampling rates of less than 50 MHz is not straightforward and will usually require some experimentation by the user in order to achieve the desired results.

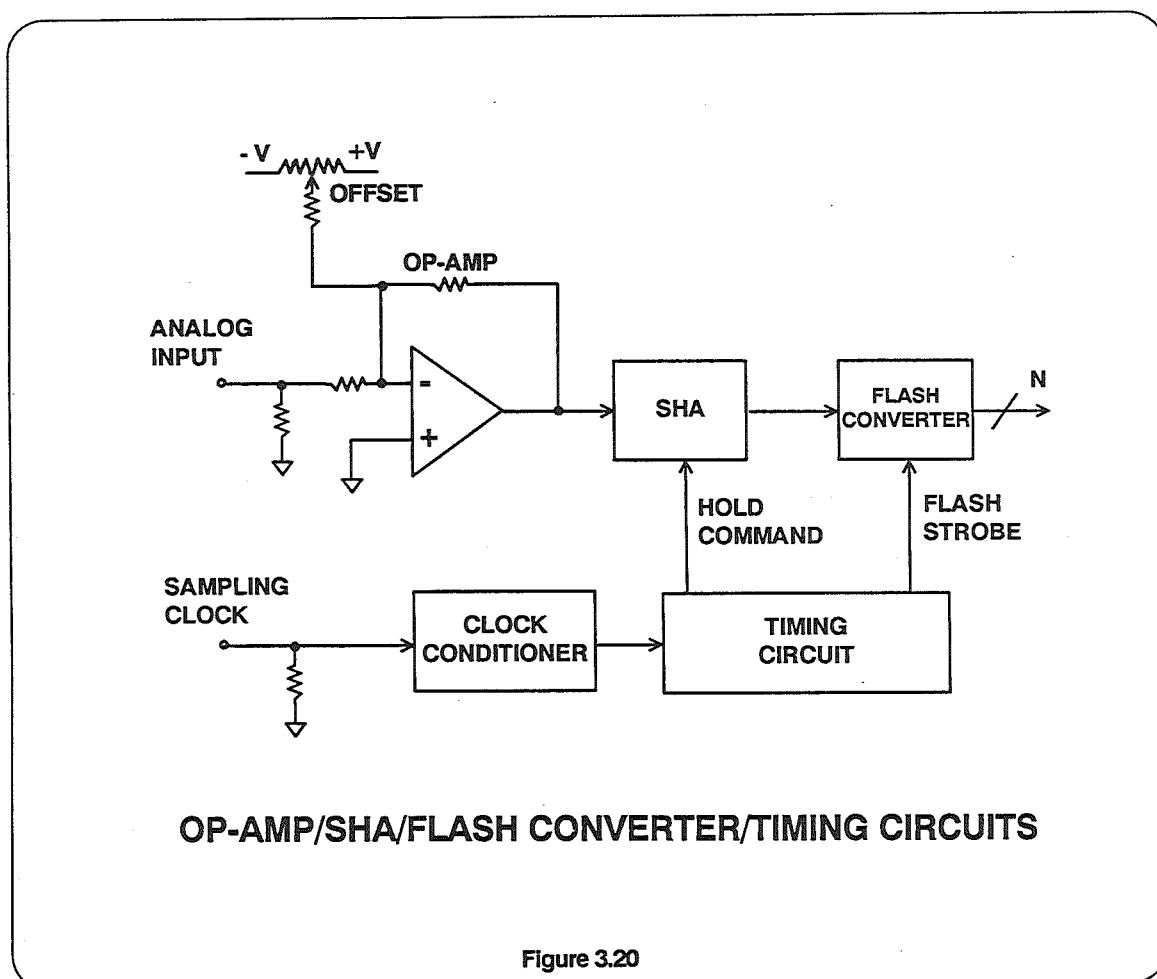
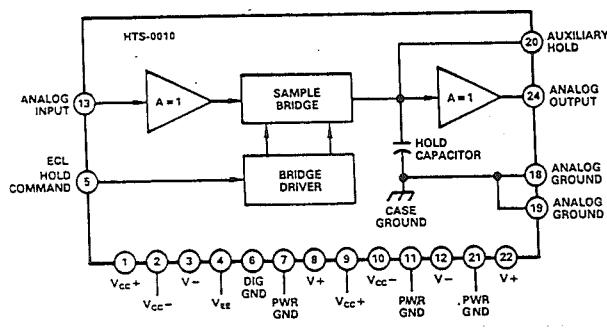
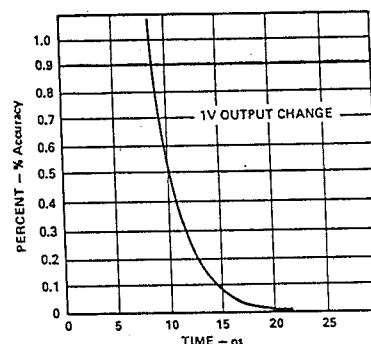


Figure 3.20



HTS-0010 BLOCK DIAGRAM



SETTLING ACCURACY VS. ACQUISITION TIME

- EFFECTIVE APERTURE DELAY TIME: -2ns
- APERTURE JITTER: 5ps RMS
- SLEW RATE: 300 V/ μ S
- INPUT RANGE: $\pm$ 3V
- FPBW = 50MHz, 2V_{p-p} INPUT
- TRACK MODE HARMONIC DISTORTION: 68dB AT 4 MHz, 2V_{p-p} INPUT

HTS-0010 SHA CHARACTERISTICS

Figure 3.21

The first step in the process is to determine the dynamic performance of the stand-alone flash converter itself - ENOBs, SNR, and harmonic distortion specifications should be available from the data sheet. If the data sheet performance is not being achieved, the user should make sure that dynamic performance degradation is not coming from the drive amplifier. The proper selection of the flash converter drive amplifier is discussed in detail in the flash converter section and the amplifier section of this seminar.

The SHA should be selected based upon acquisition time, bandwidth, aperture jitter and harmonic distortion. SHA harmonic distortion is almost always speci-

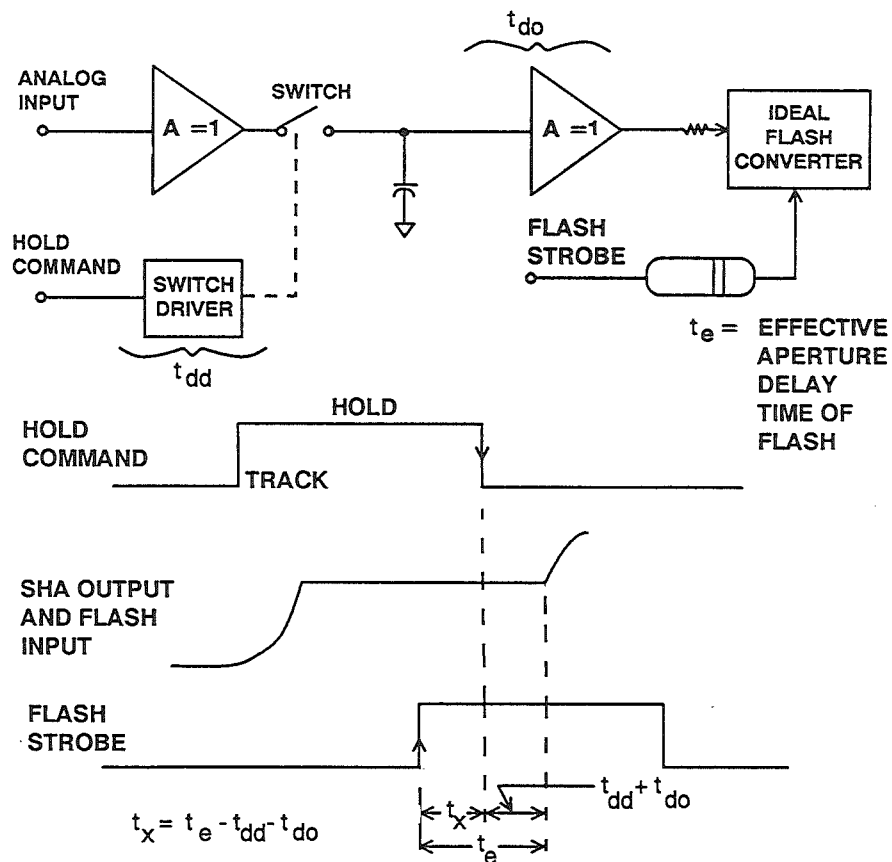
fied in the track mode and therefore may not be indicative of the performance of the SHA/flash combination. Make sure that the output voltage and drive capability of the SHA is compatible with the flash input. If level shifting is required, it should be done *ahead* of the SHA with a suitable op-amp as shown in Figure 3.20. The SHA selected will invariably have open-loop architecture such as the HTS-0010 in order to meet the acquisition time requirements. The high performance specs of the HTS-0010 hybrid SHA are given in Figure 3.21 for reference.

The most critical part of mating a SHA with a flash is the system timing. The relationship between the various pulses is

SHA/FLASH TIMING CONSIDERATIONS

- Clock Signal Conditioning If Required
- SHA Hold Command Pulse Width and Duty Cycle
- Flash Strobe Pulse Delay and Duty Cycle

Figure 3.22



SHA/FLASH TIMING RELATIONSHIPS

Figure 3.23

SHA/FLASH INTERFACING STEPS

- Select best flash converter
- Determine dynamic performance
- Select SHA (if required!)
- Determine approximate timing relationships between SHA and flash
- Design timing circuits for flexibility using ECL logic
- Optimize timing experimentally for best dynamic performance
- Check timing for adequate margin

Figure 3.24

shown in Figure 3.23. The basic system clock period is first determined by taking the reciprocal of the sampling rate. Next, choose the maximum SHA hold time based on the required acquisition time for the desired accuracy. For example, with the HTS-0010, an acquisition time of at least 15ns should be allowed for settling to 0.1% (roughly equivalent to 60 dB linearity). If the system sampling rate requirement is 25 MHz ($T = 40\text{ns}$), then a maximum hold time of 25ns is allowable (63% duty cycle). The flash strobe should be positioned as close to the end of the hold time (referenced to the SHA/flash interface) as possible. The flash effective aperture delay time (t_e), SHA switch driver delay (t_{dd}), and SHA output delay (t_{do}) can be used to determine the approximate delay time (t_x) between the trailing edge of the hold command pulse and the leading edge of the flash strobe.

In practice, both t_e and $t_{dd} + t_{do}$ are typically less than 5ns.

Figure 3.25 shows a complete SHA/flash system with ECL one-shot multivibrators (see Figure 3.26) used as pulse shapers and pulse delays. Potentiometers allow the timing to be optimized for best dynamic system performance. As an alternative to one-shots, ECL gates can be used with tapped lumped constant delay lines to generate controlled pulse widths and delays as shown in Figure 3.27. Since stable clocks are required for maximum phase and frequency stability, they often come from bipolar sources as sinewaves. A high-speed ECL comparator (such as the AD96685/96687) is useful for converting the stable sinewave into differential ECL levels while introducing a minimum of jitter as shown in Figure 3.27.

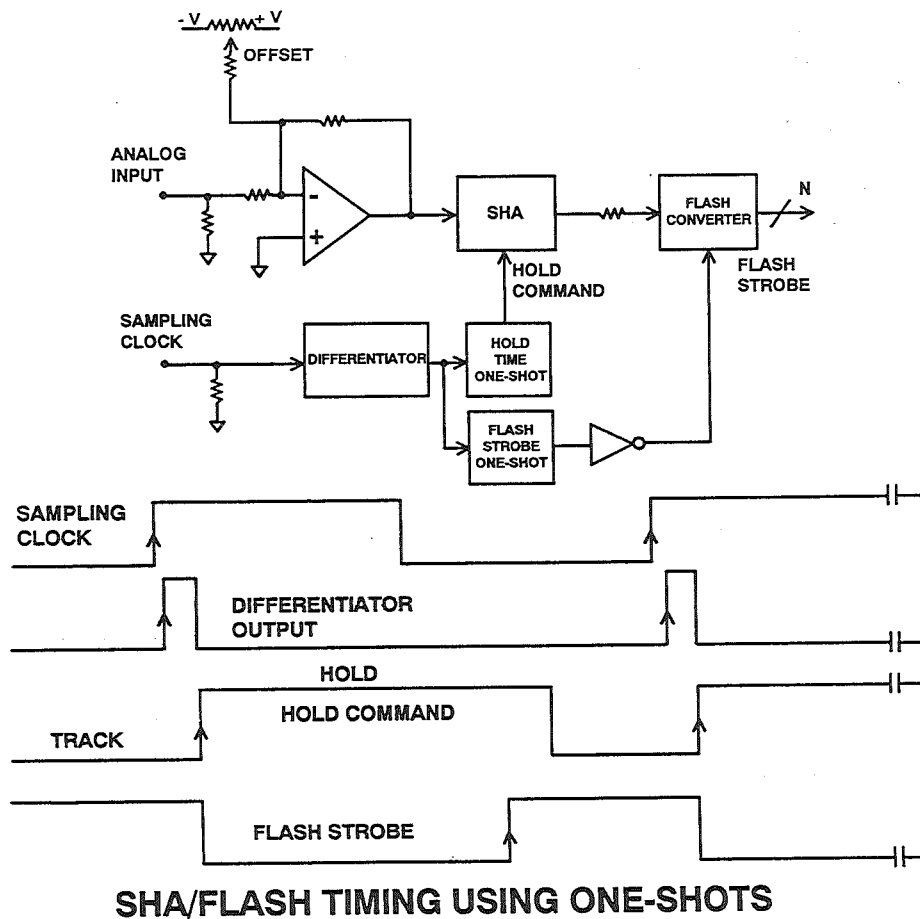


Figure 3.25

Once the optimum system timing has been determined experimentally (based on DSP analysis of the flash converter output or decimated beat frequency reconstruction), the sensitivity of the

system performance to variations in the timing pulse widths and delays should be checked to insure adequate margins have been allowed.

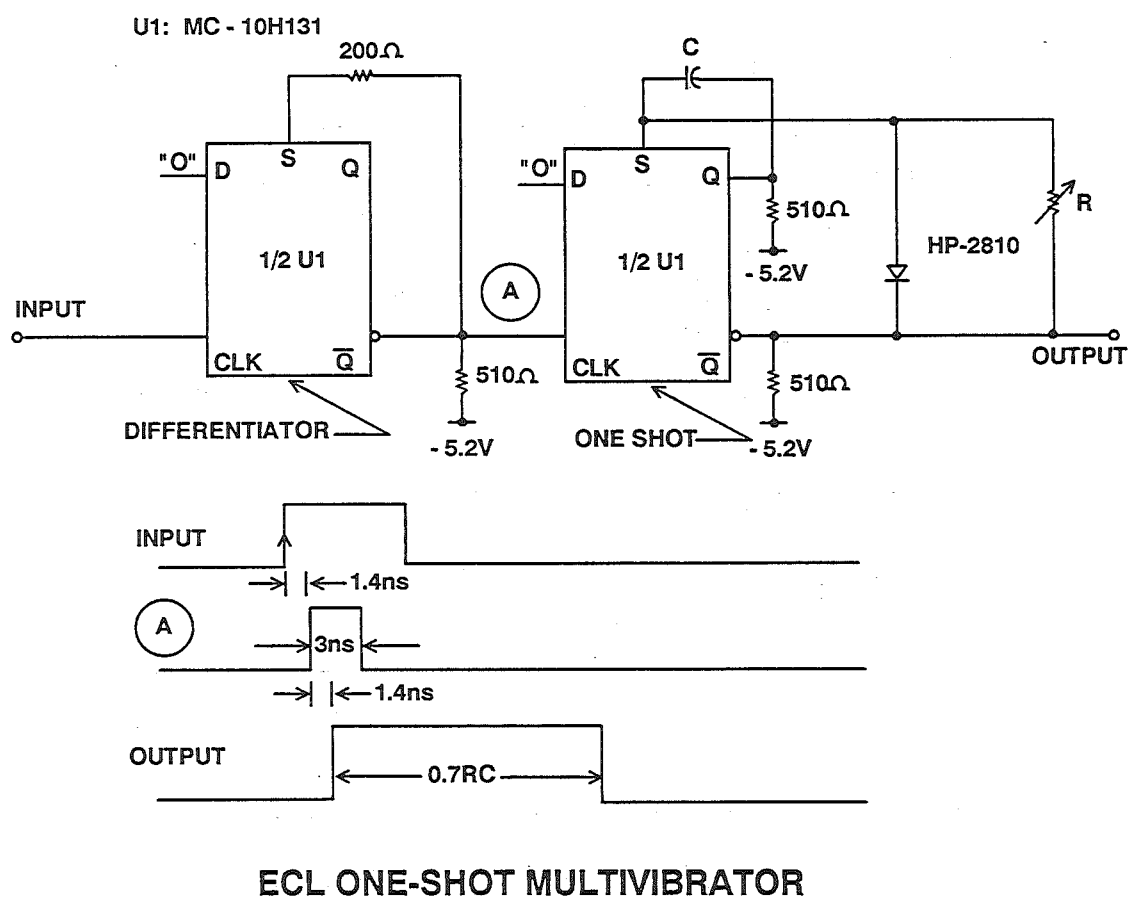
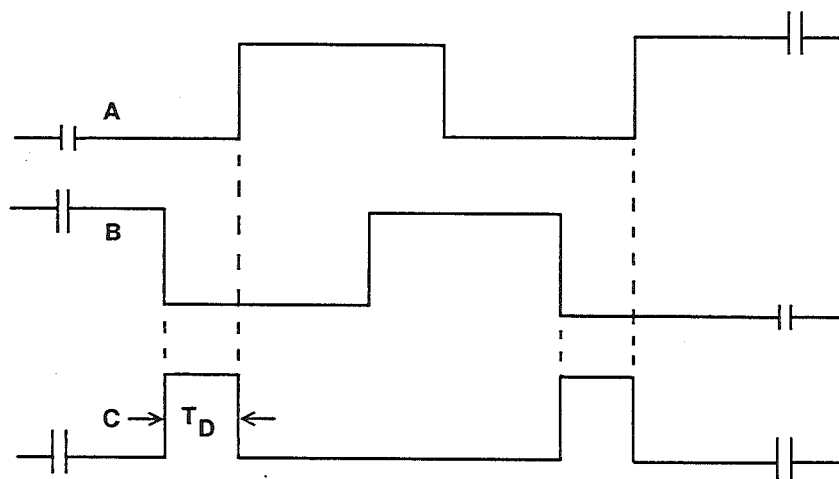
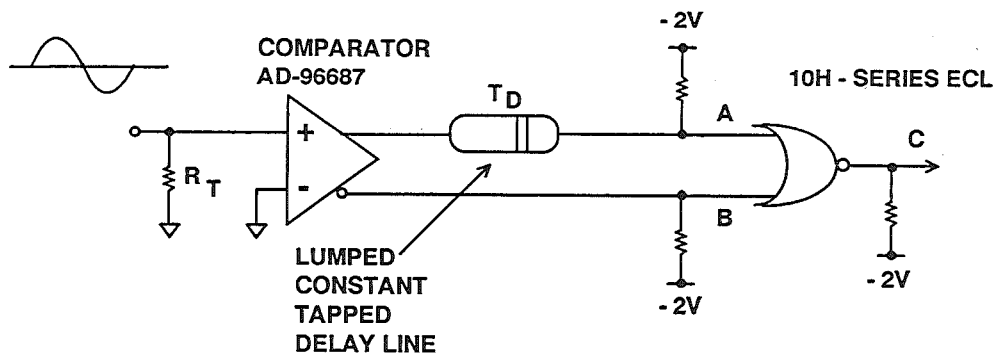


Figure 3.26



ECL PULSE CONDITIONERS

Figure 3.27

MODEL	ACQUISITION TIME	ACCURACY	APERTURE JITTER	TECHNOLOGY
HTS0010	14ns(0.1%)	0.1%	5ps	HYBRID
HTS0025	25ns(0.1%)	0.1%	20ps	HYBRID
HTC0300A	200ns(0.01%)	0.01%	50ps	HYBRID
AD346	2 μ s(0.01%)	0.01%	400ps	HYBRID
AD389	2.5 μ s(0.003%)	0.003%	400ps	HYBRID
AD386	4 μ s(16-BITS)	16-BITS	40ps	HYBRID
AD1154	3.5 μ s(16-BITS)	16-BITS	140ps	HYBRID
AD585	3 μ s(0.01%)	0.01%	500ps	IC
AD781	1 μ s(0.01%)	0.01%	50ps	IC
AD682	1 μ s(0.01%)	0.01%	50ps	DUAL AD781
AD684	1 μ s(0.01%)	0.01%	50ps	QUAD 781

SAMPLE AND HOLD SELECTION GUIDE

Figure 3.28

